

SYNTCOMP - Synthesis Competition for Reactive Systems

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We present results of the first competition for reactive synthesis tools. For this first iteration, we focused on safety specifications, which are given as sequential circuits in an extension of the AIGER format for and-inverter graphs [1]. In the extended format, input signals of the circuit can be declared as controllable or uncontrollable. The synthesized implementation can read the uncontrollable input signals, and uses this information to drive the controllable signals such that the circuit never emits a **true** value at its error output signal.

The setting allows to encode a wide range of synthesis problems, and benchmarks for the first competition ranged from machine and robot controllers to hardware components like on-chip bus arbiters, and translations of LTL properties in general. Liveness properties are encodable in the form of *bounded* liveness properties, and the competition featured both benchmarks that make and that do not make use of this approach.

Tools were ranked with respect to the time needed for realizability checks and the size of circuits produced. Particular focus has been put on the verification of the synthesized implementations. Tools had to output the resulting controller in a format that is suitable as input to tools from the hardware model checking competition (HWMCC), i.e., as another and-inverter-graph circuit. Solutions had to be verifiable by current model checking tools in order to count for the competition. The competition also featured a track in which only the realizability of a specification needed to be checked, i.e., whether some controller exists or not.

SYNTCOMP was part of the FLoC 2014 Olympic Games and relied on support by the Austrian national research network on Rigorous Systems Engineering (RiSE), funded by the Austrian Science Fund (FWF).

References

1. Swen Jacobs. Extended AIGER Format for Synthesis. In *arXiv:1405.5793*, May 2014.